AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A shift register block comprising:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits,

wherein:

a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage;

the first circuit is a second unit circuit for a second shift register different from the first shift register; and

signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers; and

~~the first circuit is not involved in operation of the first shift register so that an output of the first circuit is not supplied to any of the unit circuits of the first shift register~~.

Claim 2 (Original): The shift register block as set forth in claim 1, wherein:

the unit circuits are flip-flop circuits.

Claim 3 (Currently Amended): The shift register block as set forth in claim 1, wherein:

the first circuit includes [[is]] a processing circuit which uses output of one of the first unit circuits.

Claims 4-7 (Canceled).

Claim 8 (Currently Amended): A signal line driving circuit, comprising:

a shift register block for sequentially outputting a selection signal, so as to drive a plurality of signal lines,

wherein:

the shift register block comprises:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits, wherein a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage, the first circuit is a second unit circuit for a second shift register different from the first shift register, and signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers ~~and the first circuit is not involved in operation of the first shift register so that an output of the first circuit is not supplied to any of the unit circuits of the first shift register~~.

Claim 9 (Currently Amended): A data signal line driving circuit comprising:

a sampling section for driving a plurality of data signal lines by sampling image data from an image signal according to a selection signal sequentially outputted from a shift register block so as to transfer the image data to the data signal lines,

wherein:

the shift register block comprises:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits, wherein a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage, the first circuit is a second unit circuit for a second shift register different from the first shift register, and signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers ~~and the first circuit is not involved in operation of the first shift register so that an output of the first circuit is not supplied to any of the unit circuits of the first shift register~~.

Claim 10 (Original): The data signal line driving circuit as set forth in claim 9, wherein:

the sampling section carries out sampling of image data of divided image signals which are generated by dividing the image signal according to an alignment order of the data signal lines, the sampling section simultaneously carrying out sampling of the image data of the divided image signals.

Claim 11 (Currently Amended): The data signal line driving circuit as set forth in claim 9, wherein:

the image signal is an analog signal~~, and the first circuit comprises at least one of a waveform shaping circuit, a buffer circuit, a sampling circuit, and a level shifter circuit, which use outputs of the unit circuits~~.

Claim 12 (Currently Amended): The data signal line driving circuit as set forth in claim 9, wherein:

the image signal is a digital signal~~, and the first circuit comprises at least one of a data latch circuit, a digital/analog conversion circuit, an output circuit, a level shifter circuit, and a decoder circuit, which use outputs of the unit circuits~~.

Claim 13 (Currently Amended): A display device, comprising:

a plurality of data signal lines;

a plurality of scanning signal lines intersecting with the data signal lines;

pixels provided for each pair of the data signal lines and the scanning signal lines;

a scanning signal line driving circuit for driving the scanning signal lines; and

a data signal line driving circuit comprising a sampling section for driving a plurality of data signal lines by sampling image data from an image signal according to a

selection signal sequentially outputted from a shift register block so as to transfer the image data to the data signal lines,

wherein:

the shift register block of the data signal line driving circuit comprises:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits, wherein a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage, the first circuit is a second unit circuit for a second shift register different from the first shift register, and signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers ~~and the first circuit is not involved in operation of the first shift register so that an output of the first circuit is not supplied to any of the unit circuits of the first shift register~~.

Claim 14 (Original): The display device as set forth in claim 13, wherein:

the data signal line driving circuit and the scanning signal line driving circuit are formed on a substrate on which the pixels are formed.

Claim 15 (Original): The display device as set forth in claim 14, wherein:

the pixels, the data signal line driving circuit, and the scanning signal line driving circuit include active elements, respectively, each of which is made of a polysilicon thin film transistor.

Claim 16 (Original): The display device as set forth in claim 15, wherein:

the active elements are formed on a glass substrate at a process temperature of not more than 600°C.

Claim 17 (Currently Amended): A shift register block comprising:

a first shift register comprising a plurality of cascade-connected first unit circuits for sequentially propagating an input signal therethrough in response to a clock signal, the first unit circuits of the first shift register being linearly disposed so that physical spaces are provided between each adjacent pair of first unit circuits; wherein

respective second unit circuits for a second shift register different ~~circuits other~~ than ~~unit circuits of~~ the first shift register are disposed in the physical spaces between each respective pair of adjacent first unit circuits of the first shift register,

signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first

and second unit circuits of the first and second shift registers ~~wherein outputs from the respective other circuits are not supplied to any of the unit circuits of the first shift register~~.

Claim 18 (Previously Presented): The shift register block according to claim 17, wherein the other circuits comprise waveform processing circuits.

Claim 19 (Canceled).

Claim 20 (Previously Presented): A display device comprising the shift register block according to claim 17.

Claim 21 (Previously Presented): The shift register block as set forth in claim 1, wherein the unit circuits for the first shift register are disposed linearly with the first circuit.

Claim 22 (Previously Presented): The signal line driving circuit as set forth in claim 8, wherein the unit circuits for the first shift register are disposed linearly with the first circuit.

Claim 23 (Previously Presented): The data signal line driving circuit as set forth in claim 9, wherein the unit circuits for the first shift register are disposed linearly with the first circuit.

Claim 24 (Previously Presented): The display device as set forth in claim 13, wherein the unit circuits for the first shift register are disposed linearly with the first circuit.

Claim 25 (Currently Amended): The shift register block as set forth in claim 17, wherein the unit circuits for the first shift register are disposed linearly with the respective second unit circuits ~~other than the units circuits~~ of the first shift register.

Claims 26–28 (Canceled).

Claim 29 (New): A shift register block comprising:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits,

wherein:

a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage;

the first circuit is a processing circuit which uses output of one of the first unit circuits, a second unit circuit for a second shift register different from the first shift register, and a processing circuit which uses output of the second unit circuit of the second shift register; and

signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.

Claim 30 (New): A signal line driving circuit, comprising:

a shift register block for sequentially outputting a selection signal, so as to drive a plurality of signal lines,

wherein:

the shift register block comprises:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits, wherein a first circuit which is not one of the first unit

circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage; the first circuit is a processing circuit which uses output of one of the first unit circuits, a second unit circuit for a second shift register different from the first shift register, and a processing circuit which uses output of the second unit circuit of the second shift register; and signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.

Claim 31 (New): A data signal line driving circuit comprising:

a sampling section for driving a plurality of data signal lines by sampling image data from an image signal according to a selection signal sequentially outputted from a shift register block so as to transfer the image data to the data signal lines,

wherein:

the shift register block comprises:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits, wherein a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit

circuit of a preceding output stage and a first unit circuit of a following output stage; the first circuit is a processing circuit which uses output of one of the first unit circuits, a second unit circuit for a second shift register different from the first shift register, and a processing circuit which uses output of the second unit circuit of the second shift register; and signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.

Claim 32 (New): A display device, comprising:

a plurality of data signal lines;

a plurality of scanning signal lines intersecting with the data signal lines;

pixels provided for each pair of the data signal lines and the scanning signal lines;

a scanning signal line driving circuit for driving the scanning signal lines; and

a data signal line driving circuit comprising a sampling section for driving a plurality of data signal lines by sampling image data from an image signal according to a selection signal sequentially outputted from a shift register block so as to transfer the image data to the data signal lines,

wherein:

the shift register block of the data signal line driving circuit comprises:

at least one system of a first shift register comprising a plurality of spaced-apart, cascade-connected first unit circuits and outputting an input signal in response to a clock signal, the first shift register sequentially outputting a selection signal from output-stages comprised of the first unit circuits, wherein a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage; the first circuit is a processing circuit which uses output of one of the first unit circuits, a second unit circuit for a second shift register different from the first shift register, and a processing circuit which uses output of the second unit circuit of the second shift register; and signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.

Claim 33 (New): A shift register block comprising:

a first shift register comprising a plurality of cascade-connected first unit circuits for sequentially propagating an input signal therethrough in response to a clock signal, the first unit circuits of the first shift register being linearly disposed so that physical spaces are provided between each adjacent pair of first unit circuits; wherein

a first circuit which is not one of the first unit circuits of the first shift register is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage,

the first unit circuit is a processing circuit which uses output of one of the first unit circuits, a second unit circuit for a second shift register different from the first shift register, and a processing circuit which uses output of the second unit circuit of the second shift register, and

signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers.